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EXAMINER	
KENNEDY, ADRIAN L	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/509,086	FURBER, STEPHEN B.	
	Examiner	Art Unit	
	Adrian L. Kennedy	2121	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 September 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/29/05 and 10/25/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Examiner's Detailed Office Action

1. This Office Action is responsive to application **10/509,086**, filed **September 28, 2004**.

2. **Claims 1-31** have been examined.

Claim Rejections - 35 USC § 112

3. Claim 21 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The term "substantially" in claim 21 is a relative term which renders the claim indefinite. The term "substantially" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. The examiner takes the position that in claiming the number of decoders being "substantially equal" to the operationally beneficial number of address decoders, it is unclear whether or not the number of decoder is or isn't equal to the number of operationally beneficial number of address decoders.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an

international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 6, 16-21, 23 and 30-31 are rejected under 35 U.S.C. 102(e) as being anticipated by Ichiriu et al. (USPN 6,597,595).

Regarding claims 1:

Ichiriu et al. teaches,

A memory configuration for use in a computer system, the memory comprising

a plurality of address decoders (Column 5, Lines 16-18; "*address decoder*" and "*additional address sources (not shown) may also be provided*"; The examiner takes the position that in teaching the use of additional address sources, Ichiriu et al. anticipates the use of plurality of address decoders as claimed by the applicant.) each of which is allocated an identifier having a predetermined number of bits (The examiner takes the position that an identifier for the address decoders is inherent in the use of multiple address decoders), each bit having first and second selectable states (The examiner takes the position that the first and second selectable states for the bits are '1' and '0', and are anticipated in the invention of Ichiriu et al.), and

a data memory having a plurality of word lines (C 5, L 16-19; "*word lines*") of predetermined length (The examiner takes the position that in broadly teaching the use of valid words in Column 3, Lines 44-46, Ichiriu et al. anticipates applicant's specific claiming of using a predetermined length word.), each of the said address decoders being activatable to select one of the plurality of word lines

(C 5, L 16-18; "*address decoder 127 decodes the selected address 178 to activate one of a plurality of word lines*"), and the address decoders comprising means to receive an input address having a predetermined number of bits (The examiner takes the position that the receiving of an input address with an predetermined number of bits, is inherent in the invention of Ichiriu et al. this inherency is present in the fact that an address decoder's inputs, are fixed for each decoder, and as a result each decoder can only take addresses of a particular predefined length.) and

means to compare the identifier of an address decoder with the input address (The examiner takes the position that the "means to compare", as claimed by the applicant, is inherent in Ichiriu et al. teaching the use of a compare operation for matching the indexes (i.e. identifiers) with the words, in Column 5, Lines 22-26) wherein the memory further comprises means to activate an address decoder if at least a predetermined minimum number of bits set to the first selectable state in the input address correspond to bits set to the first selectable state in the decoder identifier (The examiner takes the position that the "means to activate an address decoder", as claimed by the applicant, is inherent in the invention of Ichiriu et al. The position is supported by Ichiriu et al. teaching the activation of an address decoder activate based on compare operation between the index and word, which is caught in Column 5, Lines 22-26, and based on a single or multiple bit-based validity value for the word, which is taught in Column 3, Lines 44-47).

Regarding claims 6:

Ichiriu et al. teaches,

> A memory configuration wherein the data memory comprises a plurality of single bit memories, such that each bit of each word line is stored in a single bit memory (The examiner takes the position that in teaching the storage of each row of the his memory contains a valid word, and that the validity value can be stored as either a single or multiple bits in Column 3, Lines 44-47, Ichiriu anticipates the applicant's claimed invention).

Regarding claims 16:

Ichiriu et al. teaches,

> A method for operating a memory for use in a computer system,
>
> the memory comprising a plurality of address decoders (Column 5, Lines 16-18; "*address decoder*" and "*additional address sources (not shown) may also be provided*"; The examiner takes the position that in teaching the use of additional address sources, Ichiriu et al. anticipates the use of plurality of address decoders as claimed by the applicant.) each of which is allocated an identifier having a predetermined number of bits (The examiner takes the position that an identifier for the address decoders is inherent in the use of multiple address decoders), each bit having first and second selectable states (The examiner takes the position that the first and second selectable states for the bits are '1' and '0', and are anticipated in the invention of Ichiriu et al.), and

a data memory having a plurality of word lines (C 5, L 16-19; "*word lines*") of predetermined length (The examiner takes the position that in broadly teaching the use of valid words in Column 3, Lines 44-46, Ichiriu et al. anticipates applicant's specific claiming of using a predetermined length word.), each of the said address decoders being activatable to select one of the plurality of word lines (C 5, L 16-18; "*address decoder 127 decodes the selected address 178 to activate one of a plurality of word lines*"),

wherein an input address having a predetermined number of bits is input to the address decoder (The examiner takes the position that the receiving of an input address with an predetermined number of bits, is inherent in the invention of Ichiriu et al. this inherency is present in the fact that an address decoder's inputs, are fixed for each decoder, and as a result each decoder can only take addresses of a particular predefined length.), the identifier of an address decoder is compared with the input address (The examiner takes the position that the comparing, as claimed by the applicant, is inherent in Ichiriu et al. teaching the use of a compare operation for matching the indexes (i.e. identifiers) with the words, in Column 5, Lines 22-26) and address decoders are activated if at least a predetermined minimum number of bits set to the first selectable state in the input address correspond to bits set to the first selectable state in the decoder identifier (The examiner takes the position that the activation of a decoder, as claimed by the applicant, is inherent in the invention of Ichiriu et al. The position is supported by Ichiriu et al. teaching the activation of an address decoder activate based on

compare operation between the index and word, which is caught in Column 5, Lines 22-26, and based on a single or multiple bit-based validity value for the word, which is taught in Column 3, Lines 44-47).

Regarding claims 17:

Ichiriu et al. teaches,

A method wherein input data is presented at a data input of the data memory and the data is written to word lines activated by the activated address decoders (The examiner takes the position that Ichiriu et al. anticipates the applicant's claimed data presentation and line activation in his teaching of the activation of word lines by an activated decoder and the inputting or outputting information from the word in Column 4, Lines 34).

Regarding claims 18:

Ichiriu et al. teaches,

A method wherein the predetermined minimum number of bits is set such that fewer than 100 address decoders are activated by any valid input address (The examiner takes the position that in broadly teaching the activation of address decoder by valid input word in Column 4, Lines 34-36 and Column 3, Lines 44-46 without citing specific number of ranges, maximum or minimums, Ichiriu et al. anticipates the applicant's specific claiming of activating fewer than 100 decoders.).

Regarding claims 19:

Ichiriu et al. teaches,

> A method wherein the predetermined minimum number of bits is set such that fewer than 50 address decoders are activated by any valid input address (The examiner takes the position that in broadly teaching the activation of address decoder by valid input word in Column 4, Lines 34-36 and Column 3, Lines 44-46 without citing specific number of ranges, maximum or minimums, Ichiriu et al. anticipates the applicant's specific claiming of activating fewer than 50 decoders.).

Regarding claims 20:

Ichiriu et al. teaches,

> A method wherein the predetermined minimum number of bits is set such that fewer than 20 and more than 11 address decoders are activated by any valid input address (The examiner takes the position that in broadly teaching the activation of address decoder by valid input word in Column 4, Lines 34-36 and Column 3, Lines 44-46 without citing specific number of ranges, maximum or minimums, Ichiriu et al. anticipates the applicant's specific claiming of activating fewer than 20 and more than 11 decoders.).

Regarding claims 21:

Ichiriu et al. teaches,

> A method for optimising the operation of a computer memory which comprises
>
> > a plurality of address decoders (Column 5, Lines 16-18; "*address decoder*" and "*additional address sources (not shown) may also be provided*"; The examiner

takes the position that in teaching the use of additional address sources, Ichiriu et al. anticipates the use of plurality of address decoders as claimed by the applicant.) each of which is allocated an identifier (The examiner takes the position that an identifier for the address decoders is inherent in the use of multiple address decoders) having a predetermined number of bits, each bit having first and second selectable states (The examiner takes the position that the first and second selectable states for the bits are '1' and '0', and are anticipated in the invention of Ichiriu et al.), and a data memory having a plurality of word lines (C 5, L 16-19; "*word lines*") of predetermined length (The examiner takes the position that in broadly teaching the use of valid words in Column 3, Lines 44-46, Ichiriu et al. anticipates applicant's specific claiming of using a predetermined length word.),

each of the said address decoders being activatable to select one of the plurality of word lines (C 5, L 16-18; "*address decoder 127 decodes the selected address 178 to activate one of a plurality of word lines*"), the memory further comprising means to receive an input address (The examiner takes the position that the receiving of an input address is inherent in the invention of Ichiriu et al. This is inherency is supported by Ichiriu et al. teaching the inputting and outputting of word lines in Column 6, Lines 36-39), and

means to activate one or more of the address decoders if a comparison between a decoder identifier and the input address exceeds a predetermined comparison threshold,

the method comprising determining an operationally beneficial number of address decoders to be activated in response to a valid input address, and configuring the comparison threshold such that a valid input address will activate a number of address decoders substantially equal to the operationally beneficial number of address decoders to be activated (The examiner takes the position that Ichiriu et al. anticipates the applicant's determining of an operational beneficial number of addresses being operated, in teaching the use of valid and non-valid words, and the use of a highest priority match register in Column 5, Lines 17-20, which only activates the address decoders for the words (i.e. input addresses) which generate the highest matches.).

Regarding claims 23:

Ichiriu et al. teaches,

A method wherein the operationally beneficial number is determined so as to allow maximum error free data recovery from the data memory (The examiner takes the position that the highest priority match method of determining which address decoders to activate, is for the purpose of minimizing error in data recovery and storage. This position is supported by Ichiriu et al. teaching that his invention is for error detection in Column 1, Lines 13-15, teaching the exclusion of error addresses in Column 7, Lines 1-8, and the matching of highest priority words in Column 5, Lines 17-21).

Regarding claims 30:

Ichiriu et al. teaches,

> A carrier medium carrying computer readable code means to cause a computer to execute procedure in accordance with the method of claim 16 (The examiner takes the position that the means claimed by the applicant is inherent in Ichiriu et al. teaching his invention carrying out his teachings.).

Regarding claims 31:

Ichiriu et al. teaches,

> A computer program for carrying out the method of claim 16 (The examiner takes the position that the program claimed by the applicant is inherent in Ichiriu et al. teaching his invention being carried out in his teachings.).

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claim 15 is rejected under 35 U.S.C. 102(b) as being anticipated by Thewes et al. (USPN 6,037,626).

Regarding claims 15:

Thewes et al. teaches,

A neural network memory configuration for use in a computer system, the memory comprising

a plurality of address decoder neurons each of which is connected to a predetermined number of input neurons (C 2, L 63 – C 3, L 3; "*the neuron input E2 and the single input electrode 7 being connected to the neuron input E4, by means of the multiplexers*"; The examiner takes the position that it is widely known in the art that an address decoder is a multiplexer.), and

a data memory having a plurality data neurons (The examiner takes the position that in teaching the receiving of data at input neurons, Thewes et al. anticipates the applicant's claimed "data neurons". This position is supported by the applicant teaching in Paragraph 0169, that the data neurons are connected to the address decoder neurons, which is anticipated by Thewes teaching the connecting of his input neurons being connected to his multiplexers (i.e. address decoders)), each of the said address decoder neurons being activatable to select some of the plurality of data neurons (The examiner takes the position that Thewes et al. anticipates the activation of decoder neurons by data neurons in teaching the controlling of multiplexers (i.e. address decoders) by their respective input neurons in Column 3, Lines 33-44.), and

the address decoder neurons comprising means to receive a signal representing a firing of an input neuron to which it is connected (The examiner takes the position that it is inherent for neurons to transmit signals by firing.),

wherein an address decoder neuron comprises means to activate data neurons if firing signals are received from at least a predetermined minimum number of input neurons to which the address decoder neuron is connected (The examiner takes the position that it is widely known in the art that a multiplexer has a certain number of inputs and outputs, and that in teaching the use of input neurons in connection with multiplexer in Column 3, Lines 33-44, Thewes et al. anticipates the applicant's claiming of a means to activate data neurons if a certain number of firing signals are received.).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 2-5, 7-12 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ichiriu et al. (USPN 6,597,595) in view of Mano (Computer System Architecture).

Regarding claims 2:

Ichiriu et al. teaches the method of claim 1, and anticipates the teaching of the comparing means considering the positional correspondence between bits. However, the examiner takes the position that Mano, better teaches the applicant's claimed invention.

Mano teaches

A memory configuration wherein the means to compare the identifier of an address decoder with the input address considers positional correspondence between bits set to the first selectable sate in the input address and bits set to the first selectable state in the decoder identifiers (The examiner takes the position that the teaching of matching of bits of a word with the bits of a key register (i.e. decoder identifier) on Pages 457-458), Mano anticipates the use of positional correspondence as a comparing means.).

It would have been obvious to one skilled in the art at the time of invention to combine the invention of Ichiriu et al. with the invention of Mano et al. for the purpose of building a memory configuration (Page 456, Paragraph 4; "*a memory unit accessed by content*").

Regarding claims 3:

Ichiriu et al. teaches the method of claim 1, and anticipates the teaching of the bits having an equal number of bits set to a selectable state. However, the examiner takes the position that Mano, better teaches the applicant's claimed invention.

Mano teaches,

A memory configuration wherein each address decoder identifier has an equal number of bits set to the first selectable state (The examiner takes the position that in teaching the comparison of bits on Page 458, Paragraph 1, Mano anticipates an equal number bits being set to a selectable state.).

It would have been obvious to one skilled in the art at the time of invention to combine the invention of Ichiriu et al. with the invention of Mano et al. for the purpose of building a memory configuration (Page 456, Paragraph 4; "*a memory unit accessed by content*").

Regarding claims 4:

Ichiriu et al. teaches the method of claim 1, and anticipates the teaching of receiving an input address containing a predetermined number of bits set to a first selectable state. However, the examiner takes the position that Mano, better teaches the applicant's claimed invention.

Mano teaches,

A memory configuration wherein the means to receive an input address is configured to receive addresses containing a predetermined number of bits set to the first selectable state (The examiner takes the position that in teaching the receiving of word with a predetermined number of bits on Page 457, and the ability of the bits to be set to either 1 (i.e. selectable) or 0 (i.e. non-selectable), Mano anticipates the applicant's claimed invention).

It would have been obvious to one skilled in the art at the time of invention to combine the invention of Ichiriu et al. with the invention of Mano et al. for the purpose of building a memory configuration (Page 456, Paragraph 4; *"a memory unit accessed by content"*).

Regarding claims 5:

Mano teaches,

A memory configuration wherein the predetermined number of bits set to the first selectable state in an input address is equal to the number of bits set to the first selectable state in each of the address decoder identifiers (The examiner takes the position that in

teaching the positional correspondence of bits on Page 457, Paragraph 3, Mano anticipates the applicant's claimed invention.).

It would have been obvious to one skilled in the art at the time of invention to combine the invention of Ichiriu et al. with the invention of Mano et al. for the purpose of building a memory configuration (Page 456, Paragraph 4; "*a memory unit accessed by content*").

Regarding claims 7:

Ichiriu et al. teaches the method of claim 1, but doesn't not explicitly teach the input line containing an equal number of bits to each of the plurality of word lines. However, the examiner takes the position that Mano, better teaches the applicant's claimed invention.

Mano teaches,

A memory configuration wherein the data memory comprises a data input line containing an equal number of bits to each of the plurality of word lines (The examiner takes the position that in teaching the use of both *n*-to-*n* decoders and *n*-to-*m* decoders on Page 43 Paragraphs 5 and 6, where *n* is the number of bits and the number of words in the *n*-to-*n* decoder, and *n* is the number of bits and *m* is the number of words and *m* is less the *n* in the *n*-to-*m* decoder, Mano anticipates use of the words being equal to the number of bits, and less than the number of bits on the input line.).

It would have been obvious to one skilled in the art at the time of invention to combine the invention of Ichiriu et al. with the invention of Mano et al. for the purpose of building a memory configuration (Page 456, Paragraph 4; "*a memory unit accessed by content*").

Regarding claims 8:

Ichiriu et al. teaches,

> A memory configuration further comprising data writing means to copy data from the data input line to word lines activated by the address decoders (The examiner takes the position that Ichiriu et al. anticipates the use of a data writing means to copy word lines activated by the decoder in teaching the activation of word lines by a decoder, and outputting or inputting information from that word in Column 4, Lines 34-39).

Regarding claims 9:

Mano teaches,

> A memory configuration wherein the data input line is configured to receive input data containing a predetermined number of bits set to the first selectable state (The examiner takes the position that that Mano anticipates the data line receiving a predetermined number of bits set to the first selected state and in teaching the use of key registers and inputs with predefined numbers of bits on Page 457, Paragraph 3 and Page 43, Paragraph 5 respectively.).

Regarding claims 10:

> Ichiriu et al. teaches the method of claim 1, including the activation of word lines based on an activation level (C 5, L 16-26; "*highest priority match*"), but does not explicitly teach the summing of the each bit of the word line.

However Mano does teach,

A memory configuration further comprising means to sum values stored at each bit of word lines activated by an address decoder to generate an activation level value for each bit (The examiner takes the position that in teaching the summing of the input bits in a decoder on Page 44, Mano anticipates the summing claimed by the applicant.).

It would have been obvious to one skilled in the art at the time of invention to combine the invention of Ichiriu et al. with the invention of Mano et al. for the purpose of building a memory configuration (Page 456, Paragraph 4; "*a memory unit accessed by content*").

Regarding claims 11:

Mano teaches,

A memory configuration further comprising means to generate an output word containing the predetermined number of bits set to the first selectable state (The examiner takes the position that in teaching the use of an n-to-m decoder and a n-to-n decoder on Page 43, he anticipates the generation of a word containing a predetermined number of bits. Additionally, the examiner takes the position that in teaching the use of key registers where a certain number of the bits in the word have to be set to the selectable state (i.e. 1), Mano anticipates the applicant's claiming of a certain number of bits being set to a selectable state in his teachings on Pages 457 and 458.).

Regarding claims 12:

Mano teaches,

A memory configuration wherein the bits set to first selectable state in the output are the predetermined number of bits having the highest activation level (The examiner takes the position that in teaching the matching of bits on Page 457, Mano et al. anticipates the applicant's claiming of bits with predetermined number of bits set to the selectable state having the "highest activation level". This position is supported by the applicant teaching in Paragraphs 0085 and 0086, that the "activation levels" are based on the number of bits set to the selectable state).

Regarding claims 22:

Ichiriu et al. teaches the method of claim 21, but doesn't not explicitly teach comparing the bits of the input address and address decoder identifiers. However, the examiner takes the position that Mano, better teaches the applicant's claimed invention.

Mano teaches,

A method wherein the comparison compares the number of bits set to the first selectable state in the input address with the number of bits set to the first selectable state in each of the address decoder identifiers (The examiner takes the position that the teaching of matching of bits of a word (i.e. input address) with the bits of a key register (i.e. decoder identifier) on Pages 457-458), Mano anticipates the comparing of the bits between the input address and address decoder identifiers.).

It would have been obvious to one skilled in the art at the time of invention to combine the invention of Ichiriu et al. with the invention of Mano et al. for the purpose of building a memory configuration (Page 456, Paragraph 4; "*a memory unit accessed by content*").

10. Claims 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ichiriu et al. (USPN 6,597,595) in view of Thewes et al. (USPN 6,037,626).

Regarding claims 13:

Ichiriu et al. teaches the method of claim 1, but does not teach the memory being implemented using a plurality of article neurons.

However, Thewes et al. teaches,

A memory configuration wherein the memory is implemented using a plurality of artificial neurons connected together to form a neural network (The examiner takes the position that in teaching the use of a plurality of neurons which are interconnected in Figure 2, Thewes et al. anticipates the applicant's claimed neural network.).

It would have been obvious to one skilled in the art at the time of invention to combine the invention of Ichiriu et al. with the invention of Thewes et al. for the purpose of creating a neuron address decoder (C 2, L 4-6; "*a respective neuron is equipped with an address decoder*").

Regarding claims 14:

Thewes teaches,

A memory configuration wherein the plurality of address decoders are represented by a plurality of address decoder neurons, and the data memory is represented by a plurality of data neurons (The examiner takes the position that Thewes et al. anticipates the

applicant's claimed plurality of address decoder being represented by address decoder neurons, in his teaching of several semiconductor neuron in Column 2, Lines 30-34, and his teaching of neuron address decoders in Column 2, Lines 4-6).

Allowable Subject Matter

11. Claims 24-29 which are not been rejected under the prior art, would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims and upon traversal of any rejections or objections found in any base claim or any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Ichiriu (USPN 6,707,693) is cited for his content addressable memory with simultaneous write and compare function. Hamalainen et al. (USPN 6,374,385) is cited for his method and arrangement for implementing convolutional decoding. Jaekel (USPN 5,113,507) is cited for his method and apparatus for a sparse distributed memory system. Ichiriu et al. (USPN 7,043,673) is cited for his content addressable memory with priority-based error detection sequencing. Srinivasan et al (USPN 6,460,112) is cited for his method and apparatus for determining a longest prefix match in a content addressable memory device. Melchior (USPN 6,473,846) is cited for his content addressable memory engine.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Adrian L. Kennedy whose telephone number is (571) 270-1505. The examiner can normally be reached on Mon -Fri 8:30am-5pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Anthony Knight can be reached on (571) 272-3687. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ALK

Anthony Knight
Supervisory Patent Examiner
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